The manufacturer
may use the marks:

Revision 2.0 August 4, 2025
Surveillance Audit Due
July 1, 2028

ANAB
ANSI National Accreditation Board
ACCREDITED
ISO/IEC 17065
PRODUCT CERTIFICATION BODY
#1004

Certificate / Certificat
Zertifikat / 合格証

Micron 21/03-104 R018

exida hereby confirms that the:

Micron Y4BM LPDDR5 SDRAM

Micron Technology, Inc.
Boise (ID), USA

Has been assessed per the relevant requirements of:

ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9

IEC 61508:2010 Parts 1 and 2

and meets the requirements providing a level of integrity to:

Systematic Capability: ASIL D / SIL 3 Capable

Random Capability: Type B, Route 1_H Device

PFH/PFD_{AVG} and Architecture Constraints must be verified for each application

Safety related function:

The Micron Y4BM LPDDR5 SDRAM is a family of memory devices targeting safety systems and applications with safety requirements up to ASIL D / SIL 3.

Application restrictions:

The Y4BM LPDDR5 SDRAM shall be used per the requirements described in the Y4BM documents listed on the reverse side.

Evaluating Assessor

Certifying Assessor

Certificate / Certificat / Zertifikat / 合格証

Micron Y4BM LPDDR5 SDRAM

ASIL D / SIL 3

Micron Y4BM LPDDR5 SDRAM

Product Overview

The Micron Y4BM LPDDR5 SDRAM is a family of memory devices compliant to the LPDDR5 JEDEC standard. The Y4BM family is based on a 12Gb silicon die, with 2, 4 or 8 dice in a single package for a total memory size of 24 to 96Gb per package. It is available in several package options, including 315 and 441-ball LFBGA / TFBGA package.

To support safety related applications, Y4BM LPDDR5 SDRAM contains several hardware safety mechanisms and design measures to prevent or to detect and control internal and external failures. Additional safety mechanisms are specified as assumptions of use, for implementation by the system integrator and user of the memory devices.

Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

The Micron Y4BM LPDDR5 SDRAM has been developed as an IC Hardware Safety Elements out of Context (SEooC) per ISO 26262-10 / Compliant Item per IEC 61508.

The development of the Y4BM SEooC, as documented by Micron, meets the applicable ASIL D requirements for specification, design, verification and validation acc. to ISO 26262 parts 4-9, as guided by ISO 26262-10, and the functional safety management requirements per ISO 26262-2, and it meets the applicable SIL 3 requirements for specification, design, verification and validation according to IEC 61508-2 and the functional safety management requirements per IEC 61508-1.

Random Hardware Integrity: Up to ASIL D / SIL 3

The FMEDA results show that Y4BM LPDDR5 SDRAM with a default set of safety mechanisms meets the ASIL C requirements and metric target values of ISO 26262-5 clause 8-9 and the SIL 2 requirements and metric target values of IEC 61508 parts 1 and 2. With an extended set of safety mechanisms (including several assumptions of use, such as error correction or error detection codes on the host controller), the Y4BM LPDDR5 SDRAM can meet the ASIL D requirements and metric target values of ISO 26262-5 clause 8-9, and the SIL 3 requirements and metric target values of IEC 61508 parts 1 and 2.

Failure rates and FMEDA metric results may have to be re-calculated and re-evaluated, based on the actual mission profile and operating conditions of the system integrating the Y4BM LPDDR5 SDRAM, and the metric targets allocated to the element within the overall system design.

The following documents are a mandatory part of this certification:

Assessment Report: Micron 21/03-104 R017, V2 R0

Safety Manual:	Automotive and Industrial LPDDR5 SDRAM
FMEDA Report:	Safety Analysis Report Automotive LPDDR5 SDRAM Safety Industrial Report Automotive LPDDR5 SDRAM

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T-048, V5R0